Distributed Sniffer Nodes for Batteryless Sensor Nodes (sdmay24-25)

Team Lead/ Software Lead: Thomas Gaul Hardware Lead: Tori Kittleson Hardware Member: Matthew Crabb Software Member: Spencer Sutton Scribe/Software Member: Ian Hollingworth

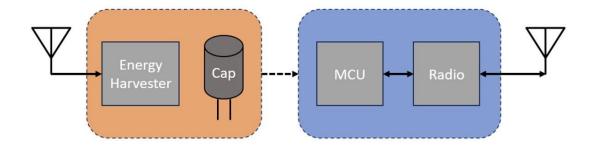
Advisor/Client: Henry Duwe CPRE/EE 492 Spring 2024



https://sdmay24-25.sd.ece.iastate.edu/ IOWA STATE UNIVERSITY

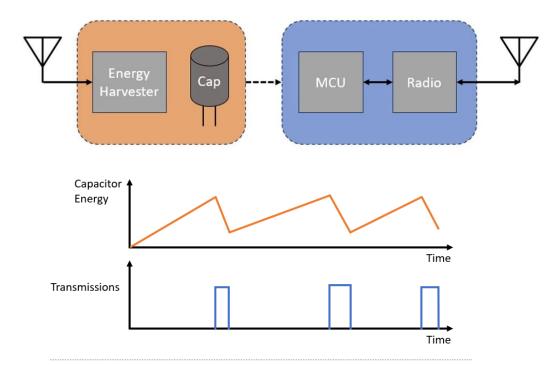
Project Overview

BOB Node - Batteryless sensor designed by client.

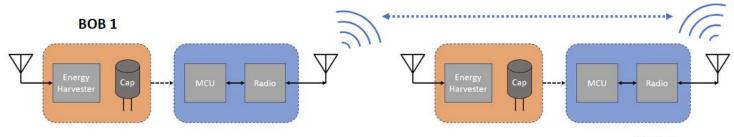


IOWA STATE UNIVERSITY

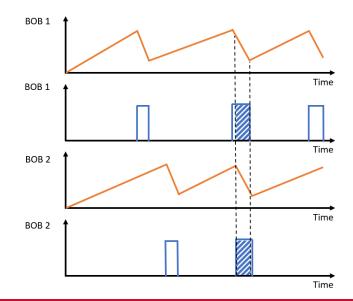
Project Overview



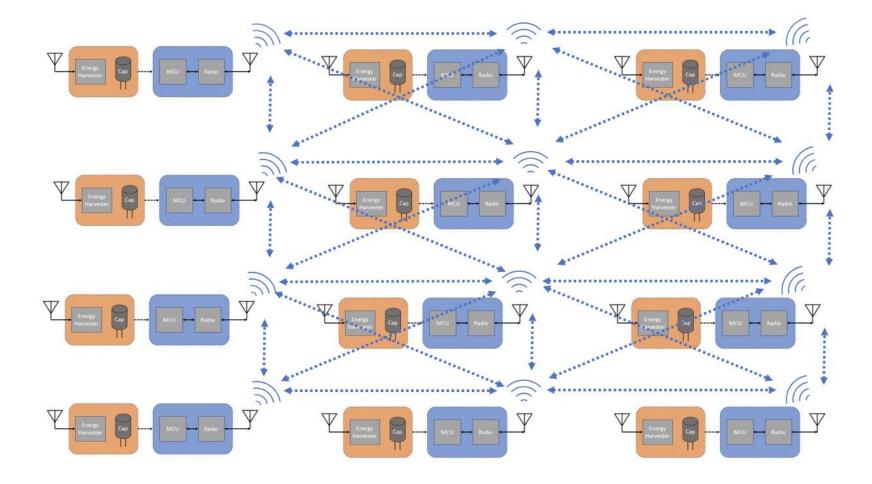
IOWA STATE UNIVERSITY





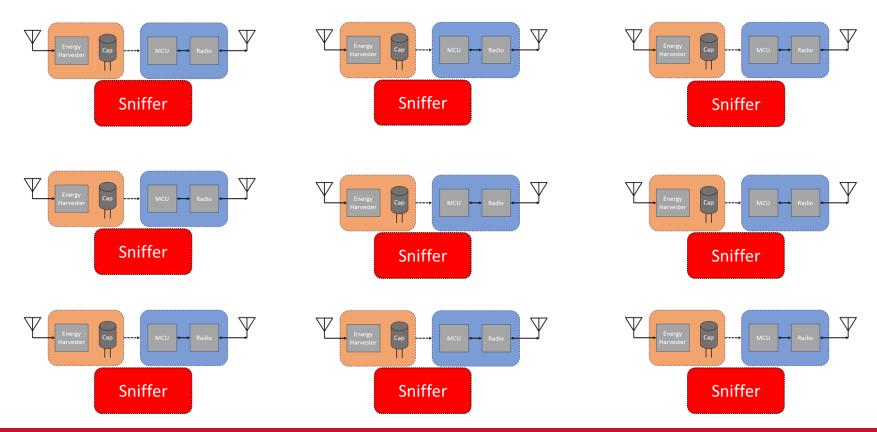


IOWA STATE UNIVERSITY



IOWA STATE UNIVERSITY

Goal: Create testbed for researchers to use for the batteryless nodes they are developing.



IOWA STATE UNIVERSITY

Use Cases

Scenario Node Tests

- Single node tests
- Multi-node and single lab testing (goal of 9)
- Large scale testing (goal of 100 1000)

Users

- Dr. Duwe's research group
- Universities, companies, hobbyists through open-source nature

Potential Impact

- Forest fire detection in national parks
- Factory condition monitoring
- Weather monitoring and recording

IOWA STATE UNIVERSITY

Requirements

Functional

- 9 BOB/Sniffer pairs
- Sink Sniffer Node with continuous power
- Host system to organize and store Sniffer logs
- Sniffer Nodes powered for one week
- Sniffer Nodes inflict minimal effects on BOB Nodes
- BOB Nodes electrically isolated from one another
- Modular stack of BOB and Sniffer custom boards

Non-functional

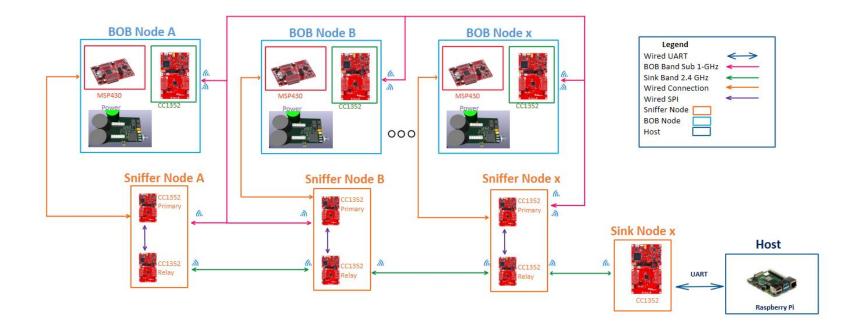
- Scalable for a potential larger (100+ node) design
- Documentation
- Mechanical durability of system

Deliverables

- Breakout Board Hardware
- MSP Simplified Hardware
- Sniffer Node Hardware
- Sniffer Node Software
- Open-Source Documentation
- Mechanically Sound System

IOWA STATE UNIVERSITY

System Design

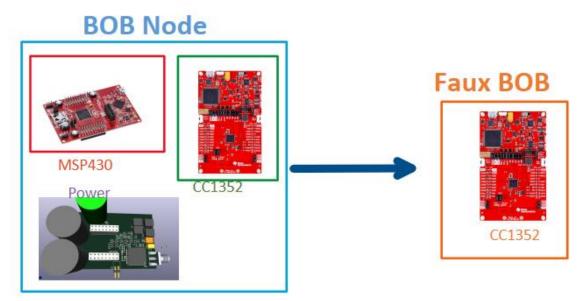


IOWA STATE UNIVERSITY

Work Progress: Faux BOB

Goal

- Create a test tool
- Emulate BOB functionality
- Allows us to have a know test



IOWA STATE UNIVERSITY

Work Progress: SPI interface

Goal

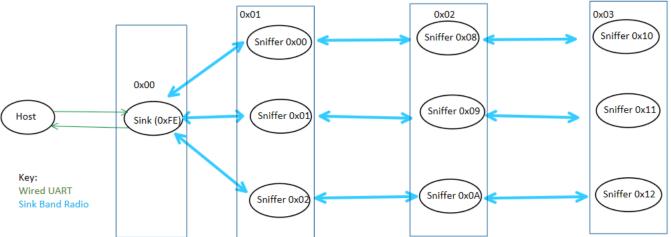
- Create interface for communicating between two CC1352s
- Allows us to take data from Band (2.4 GHz) and send it to Sub-1 GHz and vice versa

Sniffer Node C1352 Primary 1352 Relay

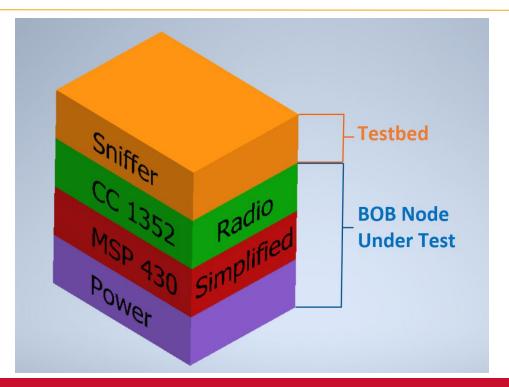
IOWA STATE UNIVERSITY

Work Progress: Software Network

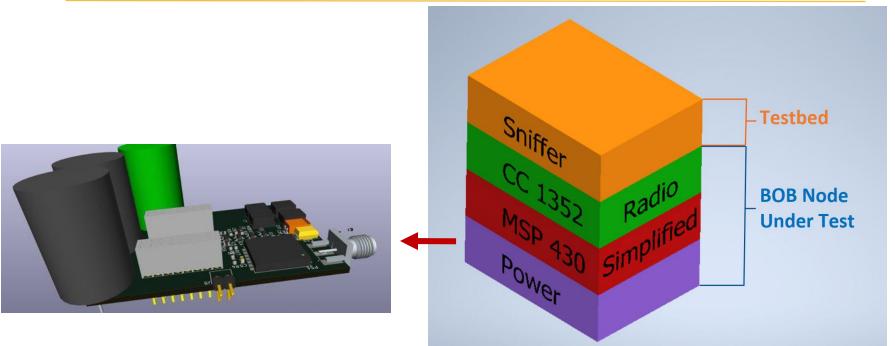
Depth Parameter Depth = [Destination Address/8] + 1 Transmit to all is 0xFF Transmit to Sink 0xF From Sink Node knows path by doing Destination % 8 Each destination is 1 byte meaning maximum of 255 destinations in the network(could be increased but due to address filtering in the BOBs this would be unnecessary unless that BOB code changes



IOWA STATE UNIVERSITY

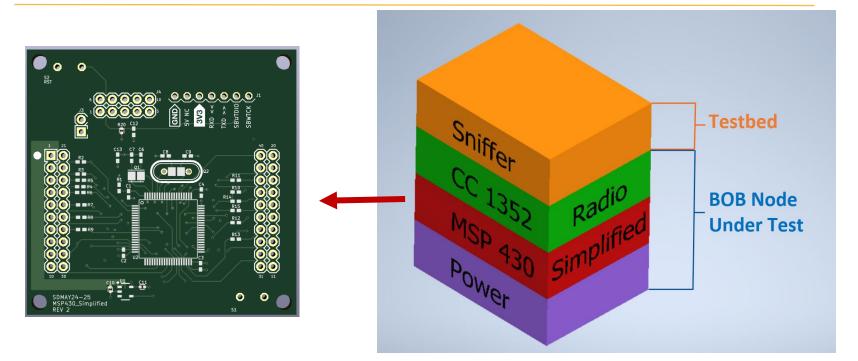


IOWA STATE UNIVERSITY



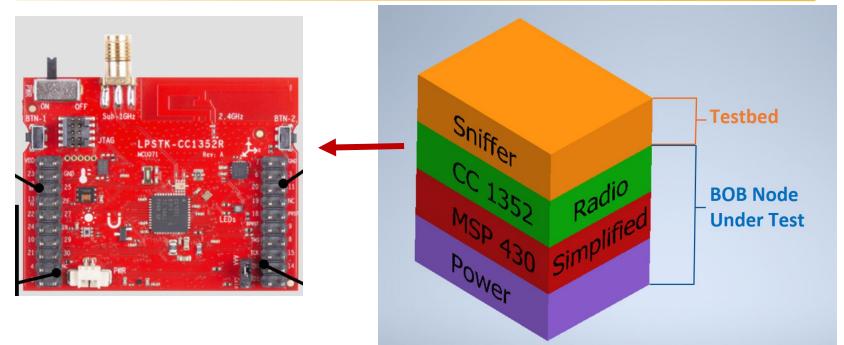
p. 27

IOWA STATE UNIVERSITY



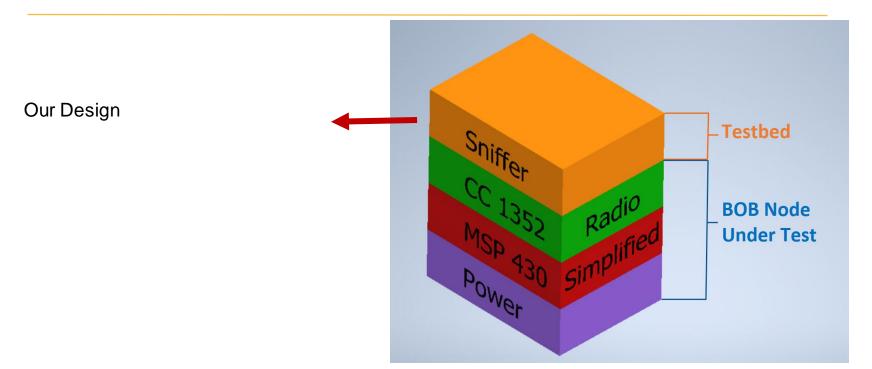


IOWA STATE UNIVERSITY

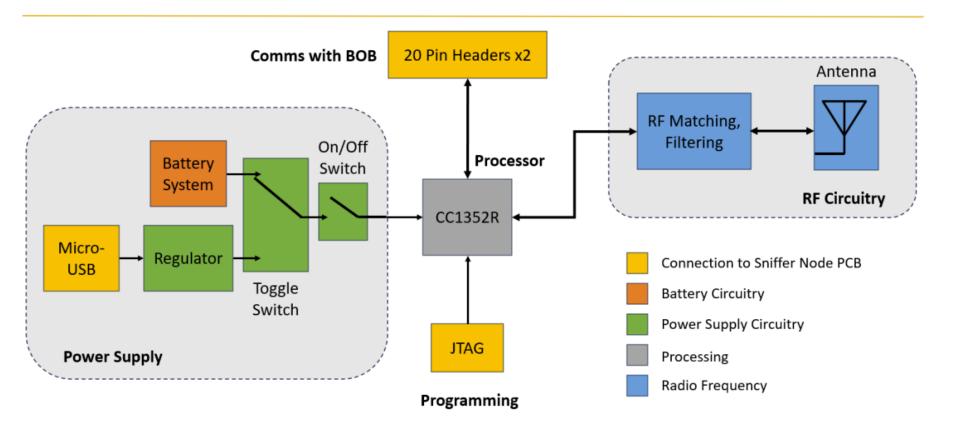


p. 27

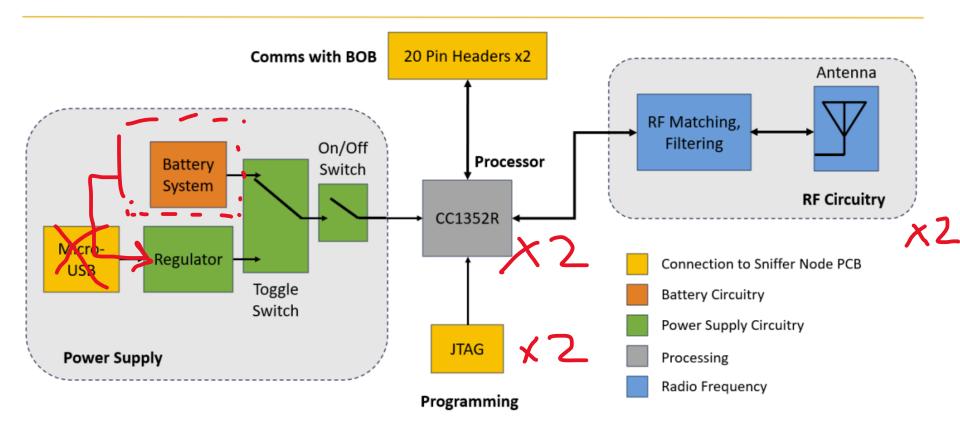
IOWA STATE UNIVERSITY



IOWA STATE UNIVERSITY



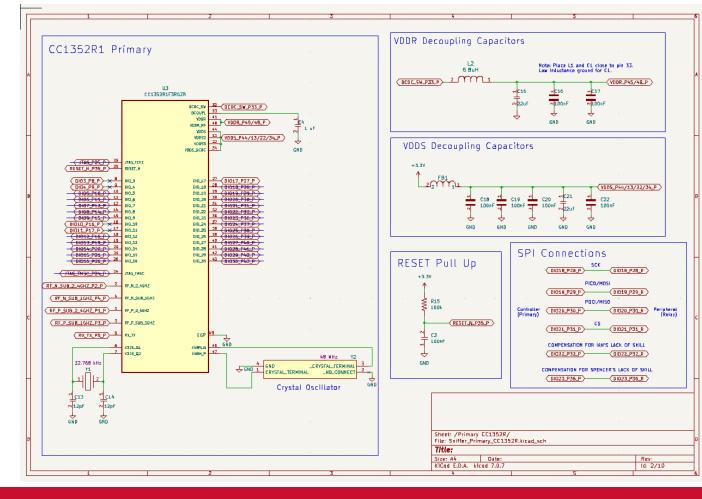
IOWA STATE UNIVERSITY



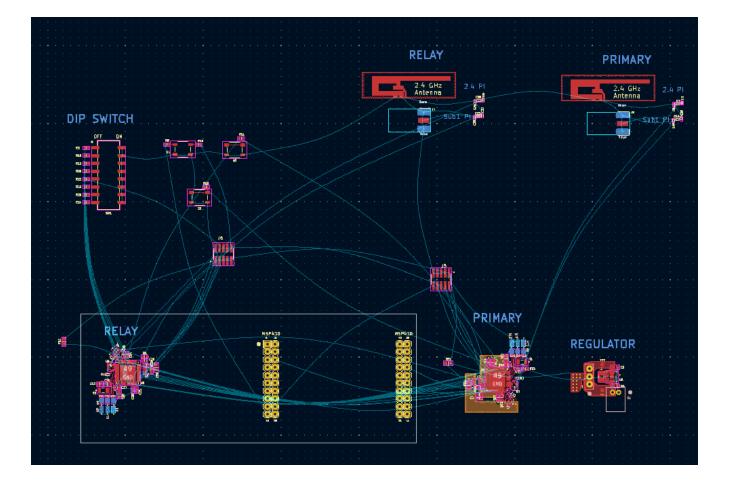
IOWA STATE UNIVERSITY

Our Design Phase:

- Schematic reviewed
- Layout In Prog

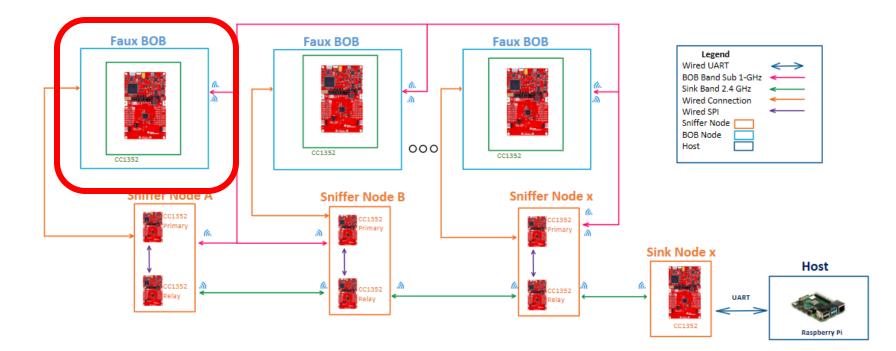


IOWA STATE UNIVERSITY



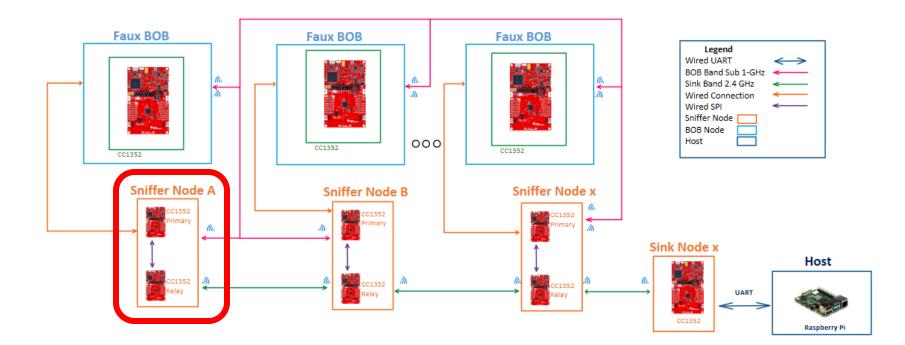
IOWA STATE UNIVERSITY

Current Software Walk-through



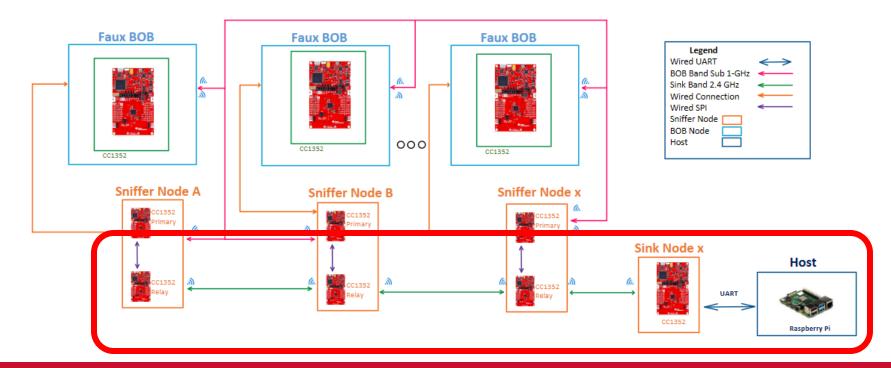
IOWA STATE UNIVERSITY

Current Software Walk-through



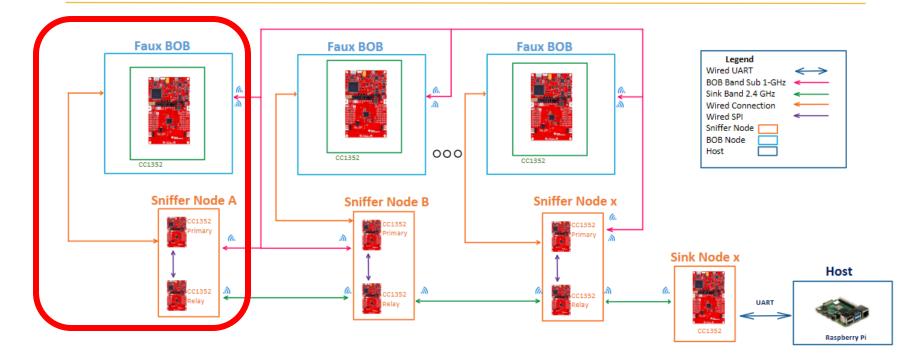
IOWA STATE UNIVERSITY

Current Software Walk-through



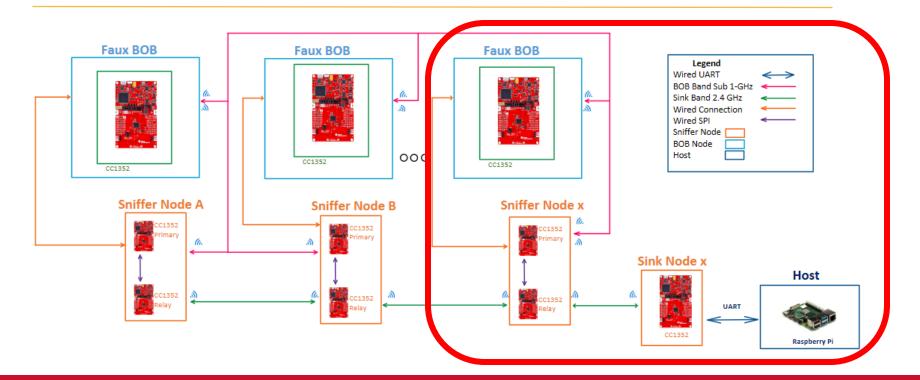
IOWA STATE UNIVERSITY

Next Step Software Walk-through



IOWA STATE UNIVERSITY

Next Steps ~90% complete



IOWA STATE UNIVERSITY

Hardware Challenges and Solutions

- → Requirement Modifications
- → Second Revision of a PCB (layout mistake)
- → Worked with client to discuss and fine tune requirements
- → Reworked PCB for a second order
- → Revised the Gantt chart to update for current progress
- → PCB Delays symbols, footprints, small details



Figure 4-1. CC1312R Board Stack Up

IOWA STATE UNIVERSITY

Software Challenges and Solutions

- → SPI integration
- → Talked to people who previously implemented it
- → Poor documentation/Weird Quirks of Software
- → Got help from experienced individuals
- → Divided up unknowns and shared knowledge

Project Plan – Schedule/Milestones

								CPR	E/EE 49	2						
	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week	Week
Project	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	16-Jan	23-Jan	30-Jan	6-Feb	13-Feb	20-Feb	27-Feb	6-Mar	Sp brk	20-Mar	27-Mar	3-Apr	10-Apr	17-Apr	24-Apr	1-May
Develop Second MSP Revision																
MSP REV 2 in fabrication																
MSP REV 2 tested and soldered																
Sniffer Design Planning							ст.									
Develop Sniffer schematic (review Tues, 27th)							Ï									
Develop Sniffer layout																
Board in Fabrication																
Test Functionality of Sniffer Hardware																
Solder MODE																
Integrate New Hardware into Test Setup																
Unit and System Testing																
Poster Design																
Panel Review Preparation																
Software Documentation																
Update Design Doc																
Full System Testing																
Faux BOB Base code																
Faux BOB "completed"																
SPI interface																
Faux BOB through SPI																
Sink Code																
Sniffer network Code																
Host Sink Sniffer relay sniffer primary Faux BOB																
2 Node setup																
2 Node deep setup																
2 Nodes with real BOB																
3 Node Deep setup																
9 Node Setup																
Dual Band																

IOWA STATE UNIVERSITY

Thank you!

Hardware Cost Estimates

Cost for	Single Board									
Item #	Designator	Manufacturer	Mfg Part #	Description / Value	Package	Supplier	Link	Qty	Cost	Total Cost
1	U1	GLF Integrated Power	GLF1111	Power Switch/Driver P-Channel 2A	SOT-23-5L	DigiKey	https://www.d	1	0.33	0.33
2	C1, C2	Samsung Electro-Mechanics	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	0402	DigiKey	https://www.d	2	0.01	0.02
3	J1	Samtec Inc.	SSW-110-03-G-D	CONN RCPT 20POS 0.1 GOLD PCB	e.	DigiKey	https://www.d	2	3.89	7.78
4	J2	Molex	22122024	TH, Right Angle 2 position 0.100" (2.54mm)	-	DigiKey	https://www.d	1	0.77	0.77
5	R1	Stackpole Electronics	RMCF0805ZT0R00	RES 0 OHM JUMPER 1/8W 0805	0805	DigiKey	https://www.d	1	0.018	0.018
6	-	-	-	Board Fabrication	-	JLCPCB	12 - 1	1	3.892	3.892
								Total Cost	t	12.48

Cost Per Breakout Board

Cost	for single board										
item #	Designator	Manufacturer	Mfg Part #	Description / Value	Package	Supplier	Link	Qty	Cost	Total Cost	
1	U1	GLF Integrated Power	GLF1111	Power Switch/Driver P-Channel 2A	SOT-23-5L	DigiKey	https://www	1	0.33	0.33	
2	C1, C2, C3, C4, C10, C11	TDK Corporation	C1005X5R1A104M050B	CAP CER 0.1UF 10V X5R 0402	0402	DigiKey	C1005X5R1/	6	0.021	0.126	
3	J2	Samtec Inc.	SSW-110-03-G-D	CONN RCPT 20POS 0.1 GOLD PCB		DigiKey	SSW-110-03	2	3.89	7.78	
4	J3	Molex	22122024	TH, Right Angle 2 position 0.100" (2.54mm)	-	DigiKey	https://www	1	0.64	0.64	
5	C6, C7	TDK Corporation	C1005C0G1H220J050BA	CAP CER 22PF 50V COG 0402	0402	DigiKey	C1005C0G1H	2	0.047	0.094	A
6	C12	TDK Corporation	C1005X7R1H102K050BA	CAP CER 1000PF 50V X7R 0402	0402	DigiKey	C1005X7R1H	1	0.051	0.051	
7	C13	Murata Electronics	GRM155R61A106ME11	CAP CER 10UF 10V X5R 0402	0402	DigiKey	GRM155R61	1	0.091	0.091	
8	J1	Sullins Connector Solution	PRPC007SBAN-M71RC	CONN HEADER R/A 7POS 2.54MM	-	DigiKey	PRPC007SB/	1	0.191	0.191	Dree
9	Q1	EPSON	FC-135R 32.7680KA-A0	CRYSTAL 32.7680KHZ 12.5PF SMD	-	DigiKey	FC-135R 32	1	0.7	0.7	Brea
10	R1, R2, R3, R4, R5, R6, R	YAGEO	RC0402JR-070RL	RES 0 OHM JUMPER 1/16W 0402	0402	DigiKey	RC0402.TR-0	17	0.0045	0.0765	
11	R18	YAGEO	RC0402FR-0747KL	RES 47K OHM 1% 1/16W 0402	0402	DigiKey	RC0402FR-0	1	0.015	0.015	
12	U2	Texas Instruments	MSP430FR5994IPN	IC MCU 16BIT 256KB FRAM 80LQFP	-	Mouser	MSP430FR59	1	11.27	11.27	MSF
13	Q2	DNP									INOI
14	-	Würth Elektronik	60900213421	JUMPER W/TEST PNT 1X2PINS 2.54MM	-	DigiKey	6090021342	1	0.31	0.31	
15	S1,S2	E-Switch	TL59NF160Q	SWITCH TACTILE SPST-NO 0.05A 12V	-	DigiKey	TL59NF1600	2	0.284	0.568	
16	J2 (trying another comp	Samtec Inc.	SSW-110-23-G-D	CONN RCPT 20POS 0.1 GOLD PCB	-	DigiKey	SSW-110-23	0	5.71	0	
17	-	-	-	PCB Fabrication	-	JLCPCB	-	1	4.96	4.96	
								Total C	ost	27.2025	

Approximate Cost Per Board							
Breakout Board	~\$13						
MSP Simplified	~\$28						

Cost Per MSP Simplified Single Board Cost

IOWA STATE UNIVERSITY

Literature Study

•"Experimental Study of Lifecycle Management Protocols for Batteryless Intermittent Communication"[2]

•"Toward a Shared Sense of Time for a Network of Batteryless, Intermittentlypowered Nodes"[3]

•"Reliable Timekeeping for Intermittent Computing"[4]



Stack Pinouts

SD)	Table 1						Table 2			
			1/O cas second frequent							
Data Received	P5.0	DIO22	I.	Powered ON	P7.7		DI025	DIO28		0
Transmit Request	P5.1	DIO3	0	Event Gen	P7.4		DIO26	DI029		I.
Transmit Done	P5.2	DIO24	I.	Testbed Reset	P7.5		DIO27	DIO30		Ē
SPI Master	P5.3	DIO19	0	Easylink Tx		DIO25	DI024	DIO21		
Ready				Event	P7.6		DI09	DIO8		0
SPI Slave Ready	P5.4	DIO7	1	Reset	P7.3				Reset	I.
FRAM Written	P5.5	DIO11	0							
Power radio	PJ.4									
SPI MOSI	P6.4	DIO9		Note on	and the last of the second		harry and		See free	
SPI MISO	P6.5	DIO8			rrently in ou nodes. I/O					
SPI CLK	P6.6	DIO10		maproo		Code need				
SPI SS	P6.7	DIO20	0							

Figure 12: Plan to Create Extra NC Pins on the CC1352R Development Board

IOWA STATE UNIVERSITY

Stack Pinouts

MSP Boar	d Pinout						
Pin #	Func	Pin #	Func	Pin #	Func	Pin #	Func
1	3V3 to CC	21	3V3	40	P5.4	20	GND
2	GPIO	22	GND	39	GPIO	19	P5.1
3	GPIO	23	NC	38	P6.7	18	P5.5
4	GPIO	24	GPIO	37	P3.5	17	GPIO/EN
5	P5.0	25	GPIO	36	GPIO	16	NC
6	P5.2	26	GPIO	35	GPIO	15	P6.4
7	P6.6 (SPI)	27	GPIO	34	RST_MSP	14	P6.5
8	P1.0	28	P7.3	33	P1.1	13	P1.6
9	P7.4	29	P7.5	32	P1.7	12	P2.6
10	P7.6	30	P7.7	31	P2.5	11	GPIO

Figure 14: MSP Simplified Pinout

IOWA STATE UNIVERSITY

Stack Pinouts

Harvester	Board P	inout					
Pin #	Func	Pin #	Func	Pin #	Func	Pin #	Func
1	NC	21	3V3	40	P5.4	20	GND
2		22	GND	39		19	P5.1
3		23	NC	38	P6.7	18	P5.5
4		24		37	P3.5	17	
5	P5.0	25		36		16	NC
6	P5.2	26		35		15	P6.4
7	P6.6	27		34		14	P6.5
8	P1.0	28	P7.3	33	P1.1	13	P1.6
9	P7.4	29	P7.5	32	P1.7	12	P2.6
10	P7.6	30	P7.7	31	P2.5	11	

Figure 15: Power Harvester Pinout

IOWA STATE UNIVERSITY

LIPO Cost Estimate (Slightly Outdated)

Item	Cost per Item	Quantity	Total Cost
LIPO	\$5.00	10	\$50.00
Battery Mount	\$3.00	10	\$30.00
Protection/Management ICs	\$0.50	10	\$5.00
Charger ICs and parts	\$1.00	10	\$10.00
Charger PCB	\$15.00	1	\$15.00

Costper board: \$11.00

Updated cost per board (no charging board): \$9.5

IOWA STATE UNIVERSITY

Time Skew Analysis

CC1352 clock was ran with constant time reporting, compared to real-time clock

Skew ended up > .005%, .01% between any given 2 nodes

Two nodes skewing in opposite directions: take 50 seconds to skew by 5 ms



Prototype Implementations - ????

No Transmit	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

Transmit every 5ms	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

 $P_{avg} = 0.5(5.99) + 0.5(26.09) = 16.04 mW$

$$E_{wk} = P_{avg}(7)(24)(60)(60) = 9.701 kJ$$

p. 37-38

IOWA STATE UNIVERSITY

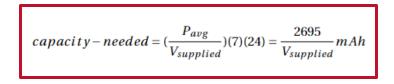
Prototype Implementations - ????

No Transmit	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

 $capacity - needed = (0.5(I_{normal}) + 0.5(I_{trans,5ms}))(7)(24)$

capacity - needed = ((0.5)(1.8152) + (0.5)(7.9060))(7)(24) = 816.581mAh

Transmit every 5ms	Min	Мах	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152



+10% buffer

p. 37-38

IOWA STATE UNIVERSITY

References

[1] "CC13xx/CC26xx Hardware Configuration and PCB Design Considerations." Accessed: Dec. 04, 2023. [Online]. Available:

https://www.ti.com/lit/an/swra640g/swra640g.pdf?ts=1701669788758&ref_url=https%253A%252F%252Fwww.google.com%252F

[2] V. Deep et al., "Experimental Study of Lifecycle Management Protocols for Batteryless Intermittent Communication," 2021 IEEE 18th International Conference on Mobile Ad Hoc and Smart Systems (MASS), Denver, CO, USA, 2021, pp. 355-363, doi: 10.1109/MASS52906.2021.00052.

[3] V. Deep, M. L. Wymore, D. Qiao and H. Duwe, "Toward a Shared Sense of Time for a Network of Batteryless, Intermittently-powered Nodes," 2022 IEEE International Performance, Computing, and Communications Conference (IPCCC), Austin, TX, USA, 2022, pp. 138-146, doi: 10.1109/IPCCC55026.2022.9894317.

[4] Jasper de Winkel, Carlo Delle Donne, Kasim Sinan Yildirim, Przemysław Pawełczak, and Josiah Hester. 2020. Reliable Timekeeping for Intermittent Computing. In Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '20). Association for Computing Machinery, New York, NY, USA, 53–67. https://doi.org/10.1145/3373376.3378464

IOWA STATE UNIVERSITY